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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,763	08/16/2001	Xiaowei Deng	TI-29320	5414

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,763	DENG, XIAOWEI	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5-7,9-11 and 13-15* is/are rejected.

7)☒ Claim(s) *8,12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *07 August 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☒ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Acknowledgement

Receipt is acknowledged of the Appeal Brief filed July 18, 2003.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "gate tied to a floating substrate body" must be shown in figures 4 (claim 4), 5 (claim 8), and 6 (claim 12) as it has been done in figure 7 (claim 16) or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tran et al. (US 5,187,686).

Regarding claim 9, Han discloses a dynamic logic circuit comprising:

a pull-down network (76) comprising a plurality of parallel connected MOS transistors with a first (B) and second (A) common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a precharge circuit (72) connected to a clock signal (CLK) and to said first common node of said pull-down network;

a ground switch circuit (74) connected to said clock signal and to said second common node of said pull-down network; and

an output node (PCHGB) which is connected to said first common node of said pull-down network.

The recitation that "on a SOI substrate" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Regarding claim 10, Han discloses that said precharge circuit comprises a PMOS transistor (421).

Regarding claim 11, Han discloses that said ground switch circuit comprises a NMOS transistor (423-2).

Claims 5-7 and 13-15 are rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Han et al (KR2001047544).

Regarding claim 5, Han discloses a dynamic logic circuit comprising:

a pull-down network (422-2) comprising a plurality of series (not shown but inherent that when NAND/AND function is desired for the PMOS logic block; for example, see 27 in Fig. 2 of Gupta et al. for series connection of transistors) connected PMOS transistors;

a precharge circuit (421, 422-1) connected to a clock signal (CK'), a circuit supply voltage (VDD), and said pull-down network (422-2);

a ground switch circuit (423-2) connected to said clock signal and to said pull-down network; and

an output node (F4) which is connected to a common node of said pull-down network and said precharge circuit.

The recitation that "on a SOI substrate" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Even if it is not inherent that the PMOS transistors of the pull-down network is connected in series, it is well known in the art that when NAND/AND function is desired for the PMOS logic block the transistors are connected in series; for example, see 27 in Fig. 2 of Gupta et al. for series connection of transistors. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided the circuit of Han et al. with series connected transistors because it is an obvious matter of design choice or substitution of equivalence.

Regarding claim 6, Han discloses that said precharge circuit comprises a PMOS transistor (421).

Regarding claim 7, Han discloses that said ground switch circuit comprises a NMOS transistor (423-2).

Regarding claim 13, Han discloses a dynamic logic circuit comprising:

a pull-down network (422-2) comprising a plurality of parallel (not shown but inherent that when NOR/OR function is desired for the PMOS logic block; for example, see 28 in Fig. 3 of Gupta et al. for parallel connection of transistors) connected PMOS transistors with a first and second common nodes (inherent for NOR/OR circuit);

a precharge circuit (421, 422-1) connected to a clock signal (CK') and to said first common node of said pull-down network (422-2);

a ground switch circuit (423-2) connected to said clock signal and to said second common node of said pull-down network; and

an output node (F4) connected to said first common node of said pull-down network.

The recitation that "on a SOI substrate" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Even if it is not inherent that the PMOS transistors of the pull-down network is connected in series, it is well known in the art that when NOR/OR function is desired for the PMOS logic block the transistors are connected in parallel; for example, see 28 in Fig. 3 of Gupta et al. for

parallel connection of transistors. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided the circuit of Han et al. with parallel connected transistors because it is an obvious matter of design choice or substitution of equivalence.

Regarding claim 14, Han discloses that said precharge circuit comprises a PMOS transistor (421).

Regarding claim 15, Han discloses that said ground switch circuit comprises a NMOS transistor (423-2).

Allowable Subject Matter

Claims 1-4 are allowed.

Claims 8, 12, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

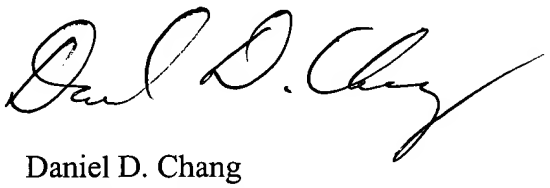
Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Daniel D. Chang
Primary Examiner
Art Unit 2819

DC
September 8, 2003

DANIEL CHANG
PRIMARY EXAMINER